



CONVITE PARA PALESTRA

Single Event Effects: Origins, Mitigation techniques and Methods & Tools for the Qualification of Digital Integrated Circuits

Dr Raoul Velazco

This talk will address radiation effects in digital circuits, mitigation techniques and a set of methods and tools to qualify digital integrated circuits under radiation.



Raoul Velazco received the MS Degree, the PhD and the Doctor ès Sciences in Computer Sciences from INPG (Institut National Polytechnique de Grenoble) in 1979, 1984 and 1990 respectively. With the CNRS (French Research Agency) since 1984, where he is Director of Researches, he leads since 1995 the "Circuit Qualification" research group at TIMA laboratory (Grenoble). His main research activities focus in the study of radiation effects on microelectronic circuits, the design hardening techniques and the development and exploitation of experiments devoted to operate on board satellites. He is the author or co-author of more than 170 publications, many of them in the prestigious IEEE Transactions on Nuclear Science. In 2001 Raoul Velazco was the general chair of the main European conference devoted to the study of the effects of radiation on integrated circuits and systems, the Radiation and their Effects in Circuits and Systems (RADECS) and was involved in the organization of many workshops and conferences related with the test of integrated circuits (DFT Defect and Fault Tolerance, Latin American Test Workshop, On-Line Test Symposium).

The ARIS (*Architectures Robustes de circuits et Systèmes Intégrés*) group directed by R. Velazco cooperates since 1988 with CNES (French Space Agency), participating with them to projects related with the study in space of the behavior of integrated circuits with respect to the effects of radiation. In 1997 was launched by NRL (Naval Research Labs) a scientific satellite with a platform aiming at evaluating the behavior of digital integrated circuits in space environment: the MPTB (Microelectronics and Photonics Testbed). The experiments developed by TIMA-QLF and CNES aimed at proving robustness of digital implementations of Artificial Neural Networks with respect to transient faults provoked by ionizing. A test platform presently under development will be part of LWS/SET project (Living With a Star, Space Environment Testbed) and is devoted to the study of the efficiency of different fault tolerance techniques implemented in a SRAM-based FPGA.

Local: INSTITUTO DE ESTUDOS AVANÇADOS - IEAv

End: Rod dos Tamoios, Km 5,5 - Torrão de Ouro - S. J. Campos, SP

Data e horário: 24 de março de 2010 das 14 às 17 horas

Coord: Dr Odair Lelis Gonzalez - Tel. (12) 3947.5501 - Cel. (12) 91242799

A inscrição deverá ser feita antecipadamente via e-mail:

odairl@ieav.cta.br

Informar: nome completo, RG e instituição

Promoção: Projeto PEICE

Patrocínio: FINEP